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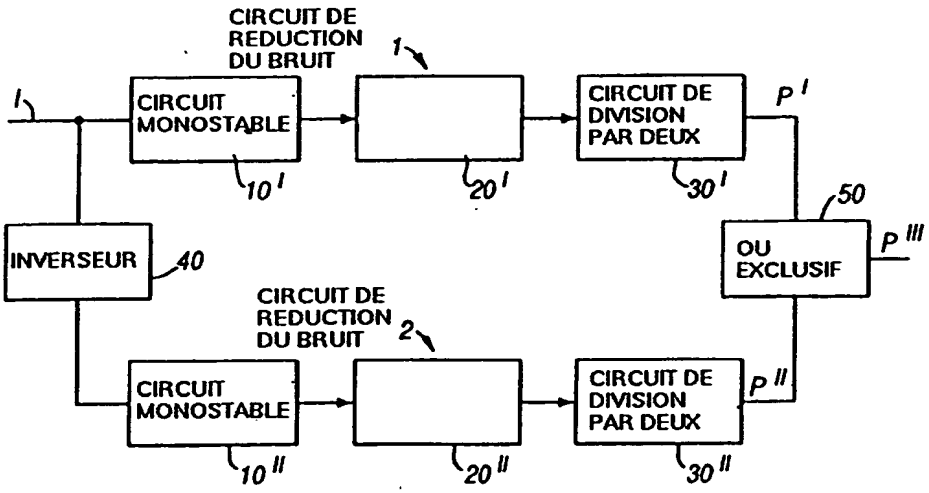

20',20'' ... CIRCUIT DE COMPENSATION DU RETARD AUTOREGLABLE

(57) Abstract

A phase noise reduction circuit for reducing phase noise in an input pulse train consisting of pulses which are all f the same length and which, in the absence of phase noise, have a nominal frequency f, includes a DC removal circuit (21) for removing a DC level from the input pulse train, or integrator (22) for integrating the input pulse train after a DC level has been removed therefrom by the DC removal circuit (21) and a comparator (23) for deriving from the integrated pulse train an output pulse train containing periodic transitions at half said nominal frequency, 1/2f. The input pulse train may be derived using a monostable circuit (10).

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PHASE NOISE REDUCTION CIRCUITS

This invention relates to phase noise reduction circuits.

The output from a frequency source, such as an oscillator or a frequency synthesiser will always contain phase noise which may be in the form of broadband noise or discrete component noise. Phase noise is undesirable in that it may ultimately limit the performance of any system (e.g. a communications or radar system) containing the frequency source. Accordingly, a low phase noise frequency source will frequently incorporate some form of compensation circuit which is designed to limit the extent of any phase noise that may be produced. However, a compensation circuit has the disadvantage that it adds to the overall complexity and expense of the frequency source.

By way of illustration, EP-A-0089721 describes a variable frequency synthesiser including a phase lock loop and a compensation circuit which is connected to the loop to reduce phase jitter therein. The compensation circuit includes an integrator and a phase modulator. The output from the integrator represents the amount of phase noise in the phase lock loop, and this output is used to control the phase modulator. The phase modulator responds to the integrator output by adjusting the relative phases of reference pulses supplied to the phase lock loop to reduce the amount of phase noise present.

According to a first aspect of the invention there is provided a phase noise reduction circuit for reducing phase noise in an input pulse train consisting of pulses which are all of the same length and which, in the absence of phase noise, have a nominal frequency f, the phase noise reduction circuit including DC removal means for removing a DC level from the input pulse train, integrator means for integrating the input pulse train after a DC level has been removed therefrom by the DC removal means, and processing means for deriving from the integrated pulse train an output pulse train containing periodic transitions at half said nominal frequency, $\frac{1}{2}f$.

According to a second aspect of the invention there is provided a phase noise reduction circuit for reducing phase noise contained in an input pulse train produced by a frequency source, which pulse train, in the absence of any phase noise, has a nominal frequency f, the phase noise reduction circuit comprising, pulse generating means for deriving a modified pulse train from the input pulse train, the modified pulse train consisting of pulses which all of the same length and are all triggered by the positive-going (or alternatively the negative-going) transitions of the pulses forming the input pulse train, and compensation means including DC removal means for removing a DC level from the modified pulse train, integration means for integrating the modified pulse train after a DC level has been removed therefrom by the DC removal means and processing means for deriving from the integrated pulse train an output pulse train containing periodic transitions at half said nominal frequency, $\frac{1}{2}f$.

According to a third aspect of the invention there is provided a phase noise reduction circuit for reducing phase noise contained in an input pulse train produced by a frequency source, which pulse train in the absence of any phase noise has a nominal frequency, f , the phase noise reduction circuit comprising a first pulse generating means for deriving a first modified pulse train from the input pulse train, the first modified pulse train consisting of pulses which are all of the same length and are triggered by the positive-going transitions of the pulses forming the input pulse train, a second pulse generating means for deriving a second modified pulse train from the input pulse train, the second modified pulse train consisting of pulses which are all of the same length and are triggered by the negative-going transitions of the pulses forming the input pulse train, first compensation means including first DC removal means for removing a DC level from the first modified pulse train, first integrator means for integrating the first modified pulse train after a DC level has been removed therefrom by the first DC removal means and first processing means for deriving from the integrated pulse train output by the first integrator means a first output pulse train containing transitions which are periodic and have the frequency $\frac{1}{2}f$, second compensation means including second DC removal means for removing a DC level from the second modified pulse train, second integrator means for integrating the second modified pulse train after a DC level has been removed therefrom by the second DC removal means and second processing means for deriving from the integrated pulse train output by the second integrator means a second output pulse train also

containing transitions which are periodic and have the frequency ½f , first and second output circuits for extracting from the first and second pulse trains respectively first and second periodic pulse trains respectively, and combining means for combining the first and second periodic pulse trains to produce a combined output pulse train at said nominal frequency f .

It will be appreciated that phase noise reduction circuits according to the invention have the capability to operate on the pulse train produced at the output of a frequency source, and need not form a part of the frequency source itself.

Embodiments of the invention are now described, by way of example only, with reference to the accompanying drawings of which,

Figure 1 shows a first phase noise reduction circuit according to the invention,

Figures 2(a) to 2(d) illustrate different waveforms useful in understanding the operation of the phase noise reduction circuit of Figure 1,

Figure 3 shows a SADC circuit forming part of the phase noise reduction circuit of Figure 1,

Figure 4 shows a second phase noise reduction circuit according to the invention, and

Figure 5 shows a specific implementation of the SADC circuit of Figure 3.

Referring now to Figure 1, the phase noise reduction circuit comprises the serial arrangement of a monostable circuit 10, a self-adjusting delay compensation (SADC) circuit 20 and a divide-by-two circuit 30.

An input pulse train I is supplied to the monostable circuit 10 via an input I/P to the phase noise reduction circuit. The input pulse train I, which may be generated by any suitable frequency source, such as an oscillator or a frequency synthesiser, has an ideal or nominal pulse repetition frequency f , but may also be subject to phase noise e.g. time jitter. The phase noise reduction circuit is designed to reduce or eliminate such phase noise.

In this embodiment, the monostable circuit 10 is triggered by the positive-going transitions in the input pulse train I (although the negative-going transitions could alternatively be used) and, in response, generates at its output a modified pulse train M consisting of pulses which all have the same, fixed length. For optimum operation of the phase noise reduction circuit, the pulses generated by the monostable circuit 10 should be shorter than the shortest pulse spacing or period in the input pulse train I, corresponding to the highest attainable input pulse repetition frequency f . In practice, the sum of the chosen pulse length and the recovery time of the monostable circuit should be less than the

shortest pulse spacing in the input pulse train I.

Figure 2(a) shows a short sequence from a modified pulse train M output by the monostable circuit 10, and demonstrates the effect of phase noise. It will be observed that the fourth pulse in the sequence is missing, resulting in an average pulse repetition frequency, f_a which is only $\frac{3}{4}$ of the nominal pulse repetition frequency f. The missing pulse is attributable to phase noise in the input pulse I and can be interpreted as a negative jump in phase by 2π in the input pulse train or a negative frequency impulse or a negative time jitter step of duration T $(= 1/f)$, corresponding to one complete cycle in the nominal pulse repetition frequency.

The modified pulse train M is supplied to the SADC circuit 20 which, as shown in Figure 3, comprises the serial arrangement of a DC removal circuit 21, an integrator 22 and a comparator 23.

Initially, the DC removal circuit 21 removes any DC component from the modified pulse train M. The resultant pulse train is then integrated by the integrator 22 and the integrator output INT is supplied to the comparator 23 where it is compared with a reference level REF. Figure 2(b) shows the integrator output INT derived from the modified pulse train M of Figure 2(a), and Figure 2(b) also shows the reference level REF with which the magnitude of the integrator output INT is compared.

The comparator 23 has a binary output and is arranged to switch this

output from one binary state (logic "1", say) to the opposite binary state (logic "0", say) whenever the magnitude of the integrator output INT crosses the reference level REF. In this manner, the comparator 23 generates an output pulse train O. Figure 2(c) illustrates the form of the output pulse train O generated by comparator 23 in response to the integrator output of Figure 2(b), and it will be observed from Figure 2(c) that each transition in the output pulse train O is coincident with a respective point of intersection of the integrator output INT and the reference level REF. The integrator output INT represents the variation of phase across the modified pulse train M, and the effect of the comparator 23 is automatically to adjust the timing of the transitions in the output pulse train O so that they all occur at the same relative phase, determined by the reference level REF. In consequence of this, the SADC circuit 20 is effective to compensate for phase noise present in the input pulse train I; however, because the pulses which form the modified pulse train M (from which the integrator output INT is derived) are all triggered by (in this embodiment) the positive-going transitions in the input pulse train I, circuit 20 is only capable of compensating for phase noise affecting the positive going transitions - in this embodiment, circuit 20 does not compensate for phase-noise affecting negative-going transitions. With this in mind, it will be seen that the (noise-compensated) positive-going pulses in the output pulse train 0 of Figure 2(c) are periodic, occurring at half the nominal pulse repetition frequency, $\frac{1}{2}f$.

The periodic, positive-going transitions correspond to the positive-going transitions in the input impulse train I after the affect of phase noise has been eliminated, and Figure 2(d) shows the corresponding noise-compensated, output pulse train P which is derived from the periodic, positive-going transitions by passing the output pulse train O of Figure 2(c) through the divide-by-two circuit 30 shown in Figure 1.

Although the SADC circuit 20 can only be used to compensate for phase noise affecting one type of transition in the input pulse train I (i.e. either positive-going transitions or negative-going transitions), it is nevertheless possible to derive a noise-compensated output pulse train having the nominal pulse repetition frequency f by passing the pulse train P (Figure 2(d)) through a frequency doubler.

In an alternative approach, two identical noise reduction circuits, each being of the form described with reference to Figures 1 to 3 may be used, and an arrangement of this kind is shown in Figure 4.

Referring to Figure 4, a first phase noise reduction circuit (NRC1) comprises the serial arrangement of a first monostable circuit 10', a first SADC circuit 20', and a first divide-by-two circuit 30'; and a second phase noise reduction unit (NRC2) comprises the serial arrangement of a second monostable circuit 10", a second SADC circuit 20" and a second divide-by-two circuit 30" . The first and second phase noise reduction circuits NRC1 and NRC2 are connected

together in parallel, and the input pulse train I (having the nominal pulse repetition frequency f) is supplied directly to the first monostable circuit 10′ and is supplied via an inverter 40 to the second monostable circuit 10".

As in the case of the embodiment described with reference to Figures 1 to 3, the first monostable circuit 10′ is triggered by positive going transitions in the input pulse train I. Therefore, the first phase noise reduction circuit (NRC1) is effective to compensate for phase noise affecting only the positive going transitions in the input pulse train I, and generates at its output a first periodic output pulse train P′ of the form shown in Figure 2(d) having half the nominal pulse repetition frequency, $\frac{1}{2}f$.

The second monostable circuit 10" is also triggered by positive-going transitions. However, because these transitions are received via the inverter 40, the second phase noise reduction circuit NRC2 is effective to compensate for phase noise affecting only the negative-going transitions in the input pulse train I. Thus, the second phase noise reduction circuit NRC2 generates at its output a second periodic output pulse train P" which is again of the form shown in Figure 2(d) but which is in phase quadrature with the first pulse train P′ generated at the output of the first phase noise reduction circuit NRC1. These two pulse trains P′, P" are combined by means of an exclusive OR device 50 to produce a phase-compensated output pulse train P‴ having the nominal pulse repetition frequency f corresponding to the input pulse train I.

Figure 5 shows a typical implementation of the SADC circuit shown in Figure 3. In this implementation, the DC removal circuit 21 comprises a capacitor C1, the integrator 22 comprises the combination of a resistor R, an operational amplifier A1 and a second capacitor C2, and the comparator 23 comprises a second operational amplifier A2 having a reference input for the reference level REF.

In practice, additional circuitry may be provided to prevent or reduce integrator drift; for example, this may be achieved by providing a small amount of resistive DC feedback between the output from and the input to the first operational amplifier A1, the amount of feedback used being insufficient to affect substantially the DC frequency response of the integrator 22.

In a modification of the embodiments described with reference to Figures 1 to 5, a feedforward signal is derived from a DC component produced at the output of the or each monostable circuit 10; 10', 10". The feedforward signal is used to offset or substantially cancel a step change in DC level occurring at the input to the or each SADC circuit 20; 20', 20" whenever the nominal pulse repetition frequency f is stepped to a new frequency, the size of the step change in DC level being dependent on the size of the frequency change. A similar offset may alternatively or additionally be achieved by means of a feedback signal derived from a DC component in the or each integrator output. If such measures are not adopted the or each SADC circuit may require an undesirably long

settling time following a large frequency step change.

An alternative modification is to use the feedforward signal to preset to a constant value the mark space ratios of the wavebands appearing at the output of the respective monostables. This has the effect of cancelling or minimising the shift in DC level to the DC removal circuit when a (large) frequency step is commanded.

In a further embodiment of the invention, two or more phase noise reduction circuits of the kind described with reference to Figures 1 to 5 may be connected together serially to form a cascaded arrangement. This enables phase noise reduction to be carried out progressively, in stages, allowing the practical design tolerance in each stage to be relaxed.

It will be appreciated that the described phase noise reduction circuits have the capability to operate on the pulse train produced at the output from a frequency source, and need not form part of the frequency source itself. A further advantage of the described circuits is that they consume relatively little power, thereby extending the potential applications of the circuits.

CLAIMS

1. A phase noise reduction circuit for reducing phase noise in an input pulse train consisting of pulses which are all of the same length and which, in the absence of phase noise, have a nominal frequency f, the phase noise reduction circuit including DC removal means for removing a DC level from the input pulse train, integrator means for integrating the input pulse train after a DC level has been removed therefrom by the DC removal means, and processing means for deriving from the integrated pulse train an output pulse train containing periodic transitions at half said nominal frequency, ½f.

2. A phase noise reduction circuit as claimed in Claim 1 wherein said processing means comprises a comparison circuit for comparing the integrated pulse train with a reference level and for generating said output pulse train as a result of the comparison.

3. A phase noise reduction circuit as claimed in Claim 2 wherein the comparison circuit generates a binary output and is arranged to switch the output from one binary state to the opposite binary state whenever the level of the integrated pulse train crosses the reference level.

4. A phase noise reduction circuit as claimed in anyone of Claims 1 to 3 further including an output circuit for extracting from said output pulse train a periodic output pulse train at said frequency, ½f .

5. A phase noise reduction circuit as claimed in Claim 4 wherein said output circuit comprises a divide-by-two circuit.

6. A phase noise reduction circuit as claimed in Claim 4 or Claim 5 including a frequency doubler for converting said periodic output pulse train at said frequency $\frac{1}{2}f$, to a periodic output pulse train at said nominal frequency f .

7. A phase noise reduction circuit for reducing phase noise contained in an input pulse train produced by a frequency source, which pulse train, in the absence of any phase noise, has a nominal frequency f, the phase noise reduction circuit comprising, pulse generating means for deriving a modified pulse train from the input pulse train, the modified pulse train consisting of pulses which all of the same length and are all triggered by the positive-going (or alternatively the negative-going) transitions of the pulses forming the input pulse train, and compensation means including DC removal means for removing a DC level from the modified pulse train, integration means for integrating the modified pulse train after a DC level has been removed therefrom by the DC removal means and processing means for deriving from the integrated pulse train an output pulse train containing periodic transitions at half said nominal frequency, $\frac{1}{2}f$.

8. A phase noise reduction circuit as claimed in Claim 7 wherein said pulse generating means comprises a monostable circuit which is triggered by said positive-going (or alternatively negative-going)

transitions of the input pulse train.

9. A phase noise reduction circuit as claimed in Claim 8 wherein the monostable circuit has an adjustable delay and produces pulses of preset length.

10. A phase noise reduction circuit as claimed in any one of Claims 7 to 9 wherein said processing means comprises a comparison circuit for comparing the integrated pulse train with a reference level, and for generating said output pulse train as a result of the comparison.

11. A phase noise reduction circuit as claimed in Claim 10 wherein the comparison circuit generates a binary output as is arranged to switch the output from one binary state to the opposite binary state whenever the integrated pulse train crosses the reference level.

12. A phase noise reduction circuit as claimed in any one of Claims 7 to 11 including an output circuit for extracting from said output pulse train a periodic output pulse train at said frequency $\frac{1}{2}f$.

13. A phase noise reduction circuit as claimed in Claim 12 wherein the output circuit comprises a divide-by-two circuit.

14. A phase noise reduction circuit as claimed in Claim 12 or Claim 13 including a frequency doubler for converting the periodic output pulse train at said frequency $\frac{1}{2}f$ to a periodic output pulse train

at said nominal frequency, f .

15. A phase noise reduction circuit for reducing phase noise contained in an input pulse train produced by a frequency source, which pulse train in the absence of any phase noise has a nominal frequency, f ,the phase noise reduction circuit comprising a first pulse generating means for deriving a first modified pulse train from the input pulse train, the first modified pulse train consisting of pulses which are all of the same length and are triggered by the positive-going transitions of the pulses forming the input pulse train, a second pulse generating means for deriving a second modified pulse train from the input pulse train, the second modified pulse train consisting of pulses which are all of the same length and are triggered by the negative-going transitions of the pulses forming the input pulse train, first compensation means including first DC removal means for removing a DC level from the first modified pulse train, first integrator means for integrating the first modified pulse train after a DC level has been removed therefrom by the first DC removal means and first processing means for deriving from the integrated pulse train output by the first integrator means a first output pulse train containing transitions which are periodic and have the frequency ½f , second compensation means including second DC removal means for removing a DC level from the second modified pulse train, second integrator means for integrating the second modified pulse train after a DC level has been removed therefrom by the second DC removal means and second processing means for deriving from the integrated pulse train output

by the second integrator means a second output pulse train also containing transitions which are periodic and have the frequency ½f, first and second output circuits for extracting from the first and second pulse trains respectively first and second periodic pulse trains respectively, and combining means for combining the first and second periodic pulse trains to produce a combined output pulse train at said nominal frequency f .

16. A phase noise reduction circuit as claimed in Claim 15 wherein said first and second pulse generating means are both monostable circuits, and the input pulse train is supplied to one or the other of the monostable circuits via an inverting circuit.

17. A phase noise reduction circuit as claimed in Claim 16 wherein the monostable circuits have adjustable delays and produce pulses of preset length.

18. A phase noise reduction circuit as claimed in anyone of Claims 15 to 17 wherein said first processing means comprises a first comparison circuit for comparing the integrated pulse train output by said first integrator means with a reference level and for generating said first output pulse train as a result of the comparison, and said second processing means comprises a second comparison circuit for comparing the integrated pulse train output by said second integrator means with a reference level and for generating said second output pulse train as a result of the comparison.

19. A phase noise reduction circuit as claimed in Claim 18 wherein the first comparison circuit generates a first binary output and is arranged to switch the first binary output from one binary state to the opposite binary state whenever the integrated pulse train output by said first integrator means crosses the reference level, and the second comparison circuit generates a second binary output and is arranged to switch the second binary output from one binary state to the opposite binary state whenever the integrated pulse train output by the second integrator means crosses the reference level.

20. A phase noise reduction circuit as claimed in anyone of Claims 15 to 19 wherein the combining means is an exclusive OR device.

21. A phase noise reduction circuit as claimed in any one of Claims 15 to 20 wherein said first and second DC removal means are responsive to a DC component produced at the output of at least one of the first and second pulse generating means whereby to reduce the effect of step a change in DC level which occurs when the nominal frequency f of the input pulse train is changed.

22. A phase noise reduction circuit as claimed in anyone of Claims 15 to 21 wherein said first and second DC removal means are responsive to feedback signals from the first and second integration means whereby to reduce the effect of a step change in DC level which occurs when the nominal frequency f of the input pulse train is changed.

23. A phase noise reduction circuit as claimed in claim 9 wherein said preset length is switched to maintain a substantially constant mark space ratio as the frequency is changed.

24. A cascaded plurality of phase noise reduction circuits as claimed in any preceding claim.

25. A phase noise reduction circuit substantially as herein described with reference to the accompanying drawings.

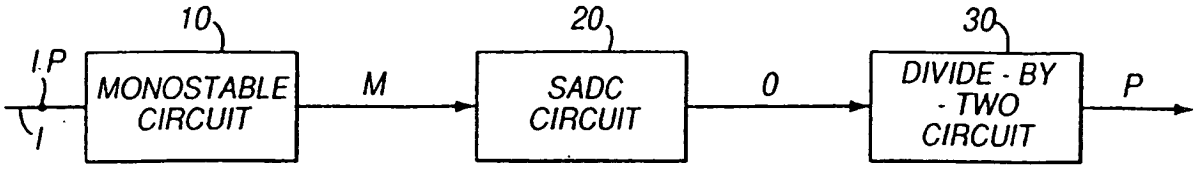

Fig. 1

Fig. 2a

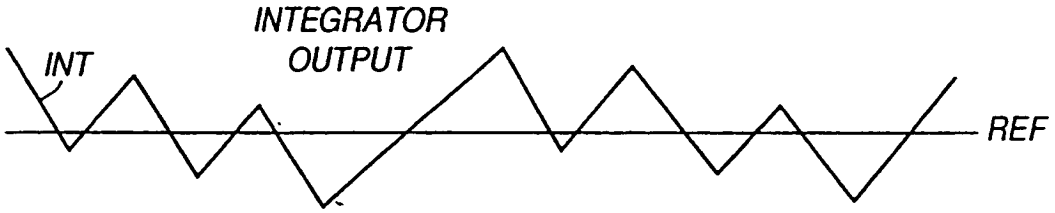

Fig. 2b

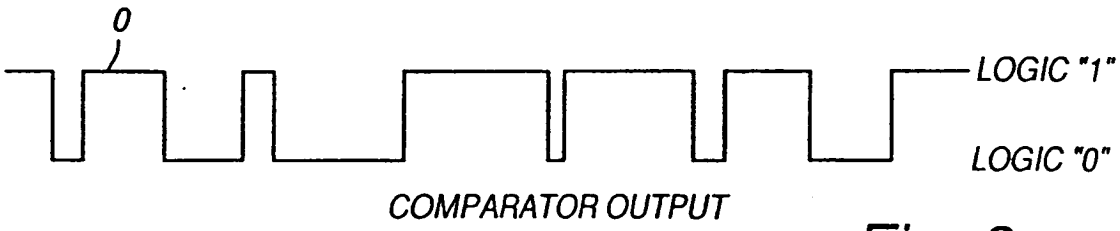

Fig. 2c

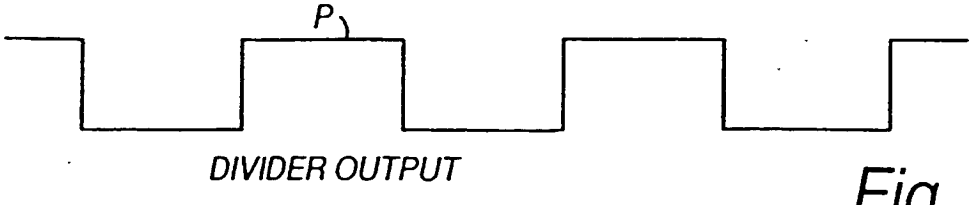

Fig. 2d

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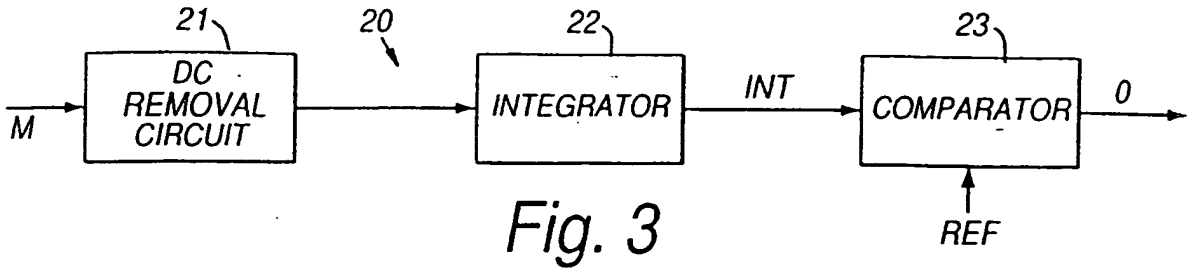

Fig. 3

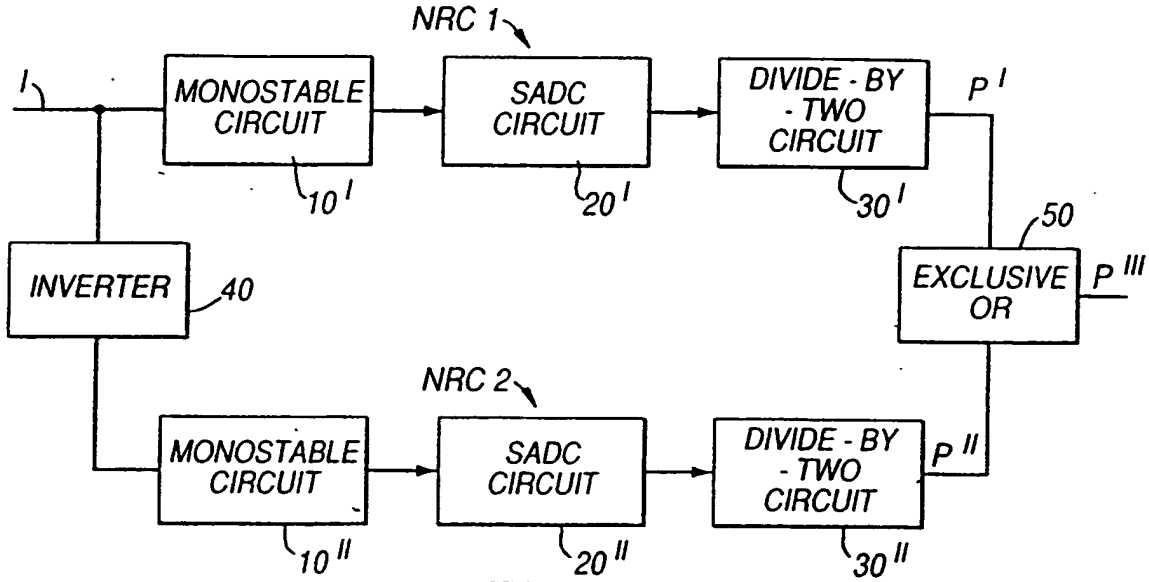

Fig. 4

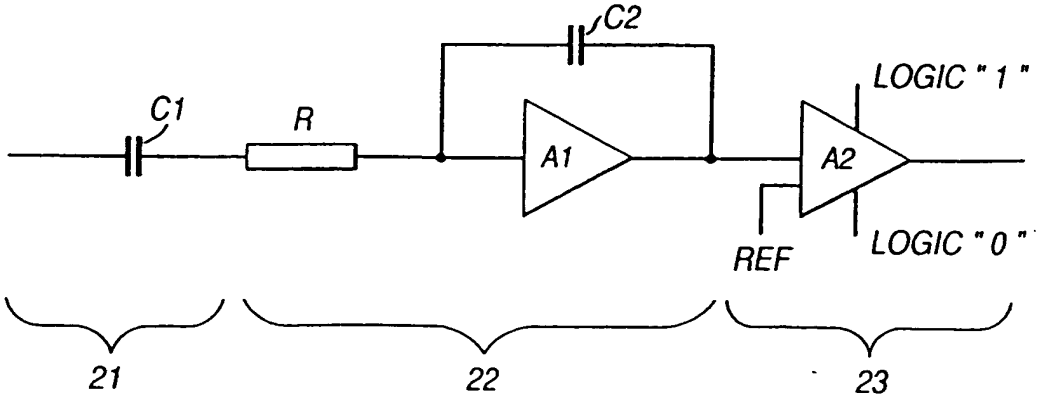

Fig. 5

INTERNATIONAL SEARCH REPORT

Inte...ational Application No
PCT/GB 97/00405

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03K5/1252

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 229 265 A (VEB GERATE) 22 July 1987 see page 5, line 7 - line 25; claims 1,3; figure 1	1
A	FR 2 578 367 A (THOMSON CSF) 5 September 1986 see page 3, line 27 - page 4, line 30; figures 1,2	1,7,15
A	US 4 137 504 A (E. SIMMONS) 30 January 1979 see column 2, line 41 - column 3, line 58; figures 1,2	1,7,15
A	US 4 780 888 A (E. SOLHJELL ET. AL.) 25 October 1988 see column 4, line 20 - column 5, line 12; figures 1,5	1,7,15

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 97/00405

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 22 12 911 A (AUGUST SAUTER KG.) 27 September 1973 see page 2, line 5 - page 4, line 11; figure 1 ---	1,7,15
A	US 5 245 557 A (E. LUPTON) 14 September 1993 see column 2, line 65 - column 3, line 66; figure 2 -----	1,7,15

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 97/00405

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 229265 A	22-07-87	NONE	
FR 2578367 A	05-09-86	NONE	
US 4137504 A	30-01-79	NONE	
US 4780888 A	25-10-88	DE 3533467 A	26-03-87
DE 2212911 A	27-09-73	NONE	
US 5245557 A	14-09-93	NONE	